

FORMING A CHIP PACKAGE
HAVING A NO-FLOW UNDERFILL

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ABSTRACT OF THE DISCLOSURE

A method of forming an underfilled chip package is provided. No-flow underfill material is deposited over a surface of a package substrate to form an underfill region. A die having a plurality of solder bumps is placed at an angle relative to the package substrate such that solder bumps adjacent a first side of the die contact the surface of the package substrate within the underfill region while solder bumps adjacent a second side of the die are generally located at a distance away from the surface of the package substrate. The second side of the die is moved toward the surface of the package substrate until the solder bumps adjacent the second side of the die contact the surface such that the underfill material is forced into the area between the plurality of bumps.